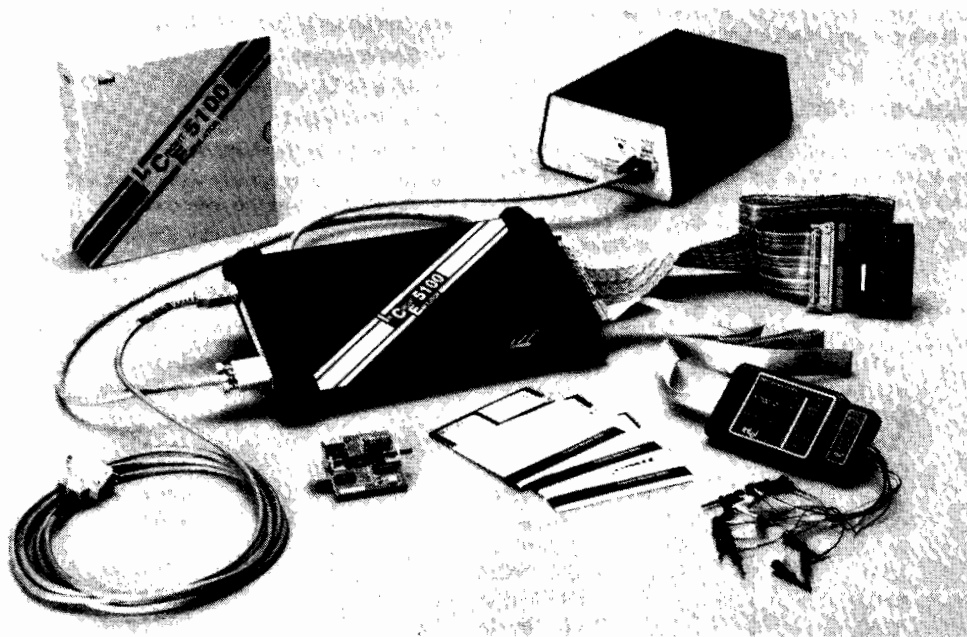




ICE™-5100/252 In-Circuit Emulator for the MCS®-51 Family of Microcontrollers

- Precise, Full-Speed, Real-Time Emulation of Selected MCS-51 Microcontroller Components at Speeds Up to and Including 16 MHz
- 64 KB of Mappable High-Speed Emulation Memory
- 254 24-Bit Frames of Trace Memory (16 Bits Trace Program Execution Addresses and 8 Bits Trace External Events)
- Serial Link to the IBM* PC AT, PC XT (and DOS Compatibles), and the Intellec® Series III/IV
- ASM-51 and PL/M-51 Language Support
- Symbolic Debugging Enables Access to Memory Locations and Program Variables
- Four Address Breakpoints with In-Range, Out-Of-Range, and Page Breaks
- Equipped with the Integrated Command Directory (ICD™) that Includes:
 - On-Line Help
 - Syntax Guidance and Checking
 - Dynamic Command-Entry
 - Error Checking
 - Command Recall
- On-Line Disassembler and Single-Line Assembler to Help with Code Patching
- Built-In CRT-Oriented Text Editor

The ICE™-5100/252 in-circuit emulator is a high-level, interactive debugging system that is used to develop and test the hardware and software of a target system based on the MCS®-51 family of microcontrollers. The ICE-5100/252 emulator can be serially linked to an IBM PC AT or PC XT, or an Intellec Series III/IV. The emulator can communicate with the host system at standard baud rates up to 19.2K. The design of the emulator supports selected MCS-51 microcontroller components at speeds up to and including 16 MHz.



*IBM is a registered trademark of International Business Machines Corporation.

280200-1

PRODUCT OVERVIEW

The ICE-5100/252 emulator provides full emulation

support for the MCS®-51 family members listed in Table 1.

The ICE-5100/252 emulator enables hardware and software development to proceed simultaneously. With the ICE-5100/252 emulator, prototype hardware can be added to the system as it is designed and software can be developed prior to the completion of the hardware prototype. Software and hardware integration can occur while the product is being developed.

The ICE-5100/252 emulator assists four stages of development:

- Software debugging
- Hardware debugging
- System integration
- System test

Software Debugging

The ICE-5100/252 emulator can be operated without being connected to the target system or before any of the user's hardware is available (provided external data RAM is not needed). In this stand-alone mode, the ICE-5100/252 emulator can be used to facilitate program development.

Hardware Debugging

The ICE-5100/252 emulator's AC/DC parametric characteristics match the microcontroller's. The emulator's full-speed operation makes it a valuable tool for debugging hardware, including time-critical serial port, timer, and external interrupt interfaces.

System Integration

Integration of software and hardware can begin

when the emulator is plugged into the microcontroller socket of the prototype system hardware. Hardware can be added, modified, and tested immediately. As each section of the user's hardware is completed, it can be added to the prototype. Thus, the hardware and software can be system tested in real-time operation as each section becomes available.

System Test

When the prototype is complete, it is tested with the final version of the system software. The ICE-5100/252 emulator is then used for real-time emulation of the microcontroller to debug the system as a completed unit.

The final product verification test can be performed using the ROM or EPROM version of the microcontroller. Thus, the ICE-5100/252 emulator provides the ability to debug a prototype or production system at any stage in its development without introducing extraneous hardware or software test tools.

PHYSICAL DESCRIPTION

The ICE-5100/252 emulator consists of the following components (see Figure 1):

- Power supply
- AC and DC power cables
- Controller pod
- Serial cable (host-specific)
- User probe assembly (consisting of the processor module and the user cable)
- Crystal power accessory (CPA)

Table 1. MCS®-51 Family Support Offered by the ICETM-5100/252 Emulator

Part	On-Chip Program Memory	On-Chip Data Memory
8031	None	128 bytes
80C31	None	128 bytes
8032	None	256 bytes
8051	4 KB-ROM	128 bytes
80C51	4 KB-ROM	128 bytes
8052	8 KB-ROM	256 bytes
80C252	None	256 bytes
83C252	8 KB-ROM	256 bytes
8751	4 KB-EPROM	128 bytes
87C51	4 KB-EPROM	128 bytes
8752	8 KB-EPROM	256 bytes
87C252	8 KB-EPROM	256 bytes

- 40-pin DIP target adaptor
- Clips assembly
- Software (includes the ICE-5100/252 emulator software, diagnostic software, and tutorial)

The controller pod contains 64 KB of emulation memory, 254- by 24-bit frames of trace memory, and the control processor. In addition, the controller pod houses a BNC connector that can be used to connect up to 10 multi-ICE compatible emulators together for synchronous starting and stopping of emulation.

The serial cable connects the host system to the controller pod. The serial cable supports a subset of the RS-232C signals.

The user probe assembly consists of a user cable and a processor module. The processor module houses the emulation processor and the interface logic. The target adaptor connects to the processor module and provides an electrical and mechanical interface to the target microcontroller socket.

The crystal power accessory (CPA) is a small detachable board that connects to the controller pod and enables the ICE-5100/252 emulator to run in

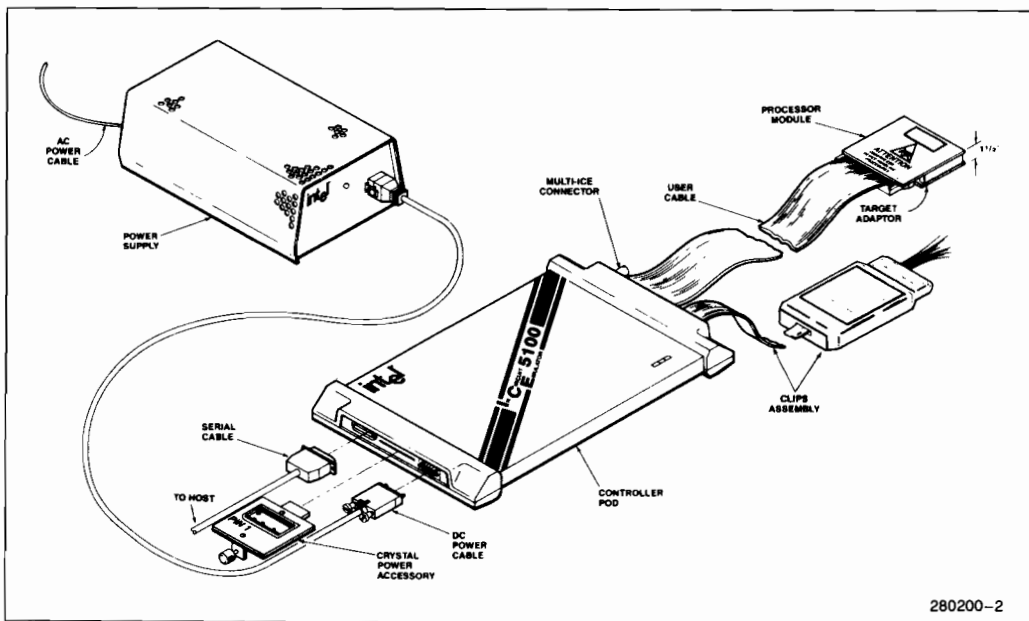
stand-alone mode. The target adaptor plugs into the socket on the CPA; the CPA then supplies clock and power to the user probe.

The clips assembly enables the user to trace external events. Eight bits of data are gathered on the rising edge of PSEN during opcode fetches. The clips information can be displayed using the CLIPS option with the PRINT command. Trace qualification input and output lines are also provided on the clips pod for connection to test equipment.

The ICE-5100/252 emulator software supports mnemonics, object file formats, and symbolic references generated by Intel's ASM-51 and PL/M-51 programming languages. Along with the ICE-5100/252 emulator software is a customer confidence test disk with diagnostic routines that check the operation of the hardware.

The on-line tutorial is written in the ICE-5100 command language. Thus, the user is able to interact with and use the ICE-5100/252 emulator while executing the tutorial.

A comprehensive set of documentation is included with the ICE-5100/252 emulator.



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Figure 1. The ICE™-5100/252 System Hardware

ICETM-5100/252 EMULATOR FEATURES

The ICE-5100/252 emulator has been created to assist a product designer in developing, debugging, and testing designs incorporating the MCS®-51 family of microcontrollers. The following sections detail some of the ICE-5100/252 emulator features.

Processor Selection

The ICE-5100/252 emulator emulates the microcontrollers listed in Table 1. Selecting a processor type changes the following characteristics to match the microcontroller selected:

- Internal RAM size
- Internal ROM size
- Idle and power down mode enable
- Special function register symbolic map
- Memory map
- Latched or unlatched \overline{EA}
- Serial port framing and error detection

Emulation

Emulation is the controlled execution of the user's software in the target hardware or in an artificial hardware environment that duplicates the microcontroller of the target system. Emulation is a transparent process that happens in real-time. The execution of the user software is facilitated with the ICE-5100/252 command language.

Memory Mapping

There is 64 KB of memory that can be mapped to the CODE memory space in 4 KB blocks on 4 KB boundaries. By mapping memory to the ICE-5100/252 emulator, software development can proceed before the user hardware is available.

Memory Examination and Modification

The memory space for the MCS®-51 component(s) and its target hardware is fully accessible through the emulator. The ICE-5100/252 emulator refers to four physically distinct memory spaces, as follows:

- CODE — references program memory
- IDATA — references internal data memory
- RDATA — references special function register memory
- XDATA — references external data memory

ICE-5100/252 emulator commands that access memory use one of the special prefixes (e.g., CODE) to specify the memory space.

The microcontroller's special function registers and register bits can be accessed mnemonically (e.g., DPL, TCON, CY) with the ICE-5100/252 emulator software.

Data can be displayed or modified in one of three bases: hexadecimal, decimal, and binary. Data can also be displayed or modified in one of two formats: ASCII and unsigned integer. Program code can be disassembled and displayed as ASM-51 assembler mnemonics. Code can be modified with standard ASM-51 statements using the built-in single-line assembler.

Symbolic references can be used to specify memory locations. A symbolic reference is a procedure name, line number, program variable, or label in the user program that corresponds to a location.

Some typical symbolic functions include:

- Changing or inspecting the value of a program variable by using the symbolic name to access the memory location.
- Defining break and trace events using symbolic references.
- Referencing variables as primitive data types. The primitive data types are ADDRESS, BIT, BOOLEAN, BYTE, CHAR (character), and WORD.

The ICE-5100/252 emulator maintains a virtual symbol table (VST) for program symbols. A maximum of 61 KB of host memory space is available for the VST. If the VST is larger than 61 KB, the excess is stored on available host system disk space and is paged in and out as needed. The size of the VST is limited only by the disk capacity of the host system.

Breakpoint Specifications

Breakpoints are used to halt a user program in order to examine the effect of the program's execution on the target system. The ICE-5100/252 emulator supports three different types of break specifications:

- Specific address break — A single address can be specified to halt emulation.

- Range break — An arbitrary range of addresses can be specified to halt emulation. Program execution within or, optionally, outside the range halts emulation.
- Page break — Up to 256 page breaks can be specified. A page break is defined as a range of addresses that is 256-bytes long and begins on a 256-byte address boundary.

Break registers are user-defined debug definitions used to create and store breakpoint definitions. Break registers can contain multiple breakpoint definitions and can optionally call debug procedures when emulation halts.

Trace Specifications

Tracing can be triggered using specifications similar to those used for breaking. Normally, the ICE-5100/252 emulator traces program activity while the user program is executing. With a trace specification, tracing can be triggered to occur only when specific conditions are met during execution. Up to 254 24-bit frames of trace information are collected in the buffer during emulation. Sixteen of the 24 bits trace instruction execution addresses, and 8 bits capture external events (CLIPS).

The trace buffer display is similar to an ASM-51 program listing shown in Figure 2. The PRINT command enables the user to selectively display the contents of the trace buffer. The user has the option of displaying the clips information as well as disassembled instructions.

Procedures

Debugging procedures (PROCs) are a user-named group of ICE-5100/252 emulator commands that are executed as one command. PROCs enable the user to define several commands in a named block structure. The commands are executed by entering the name of the PROC. The PROC bodies are a simple DO...END construct.

PROCs can simulate missing hardware or software, collect debug information, and execute high-level software patches. PROCs can be copied to text files on disk, then recalled for use in later test sessions. PROCs can also serve as program diagnostics, implementing ICE-5100/252 emulator commands or user-defined definitions for special purposes. PROCs can also be used to set breakpoints.

On-Line Syntax Menu

A special menu, called the Integrated Command Directory (ICD), similar to the one used for the I²CETM system and the VLSiCE-96 emulator, aids in creating syntactically correct command lines. Figure 3 shows an example of the ICD and how it changes to reflect the options available for the GO command.

Help

The HELP command provides ICE-5100/252 emulation command assistance via the host system terminal. On-line HELP is available for the ICE-5100/252 emulator commands shown in Figure 4.

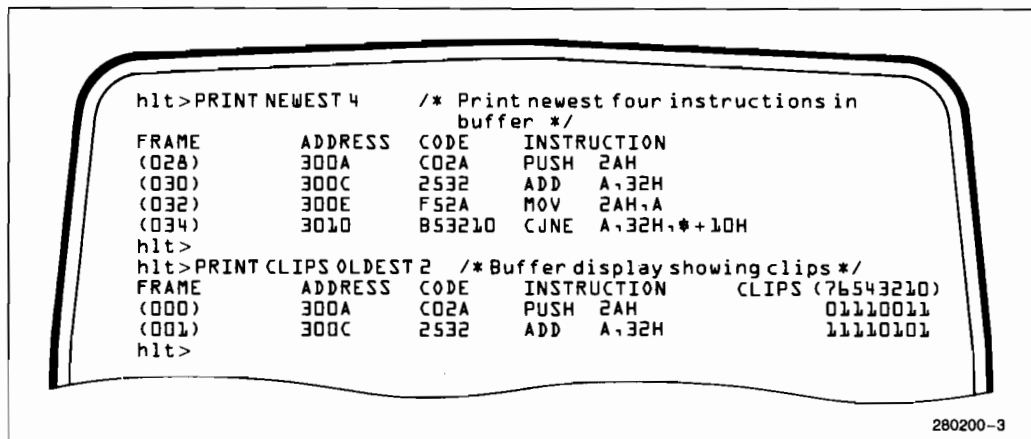


Figure 2. Selected Trace Buffer Displays

Design Considerations

The height of the processor module and the target adaptor need to be considered for target systems.

Allow at least 1-1/2 inches (3.8 cm) of space to fit the processor module and target adaptor. Figure 5

shows the dimensions of the processor module.

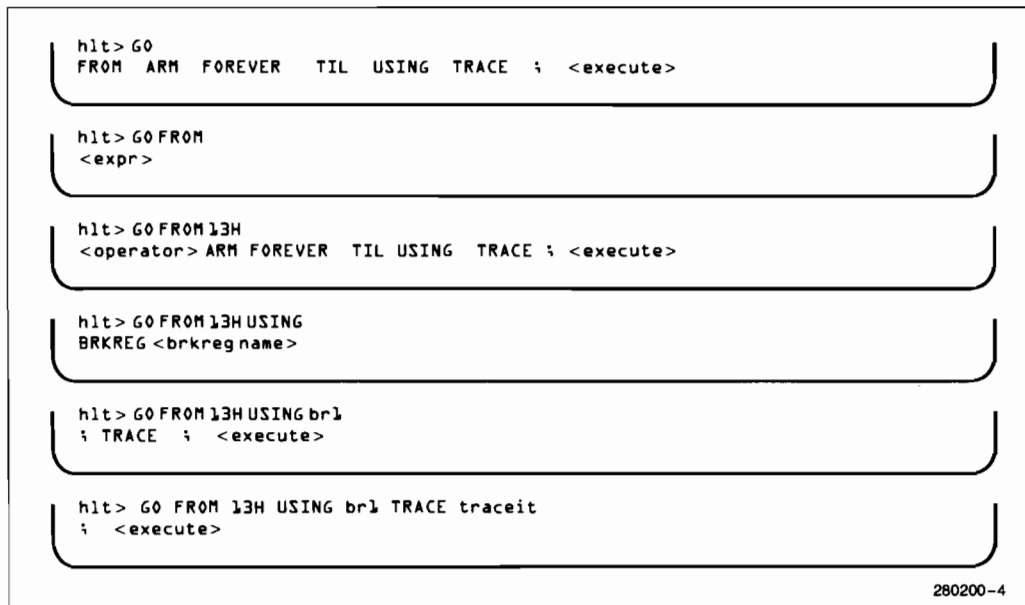


Figure 3. The Integrated Command Directory for the GO Command

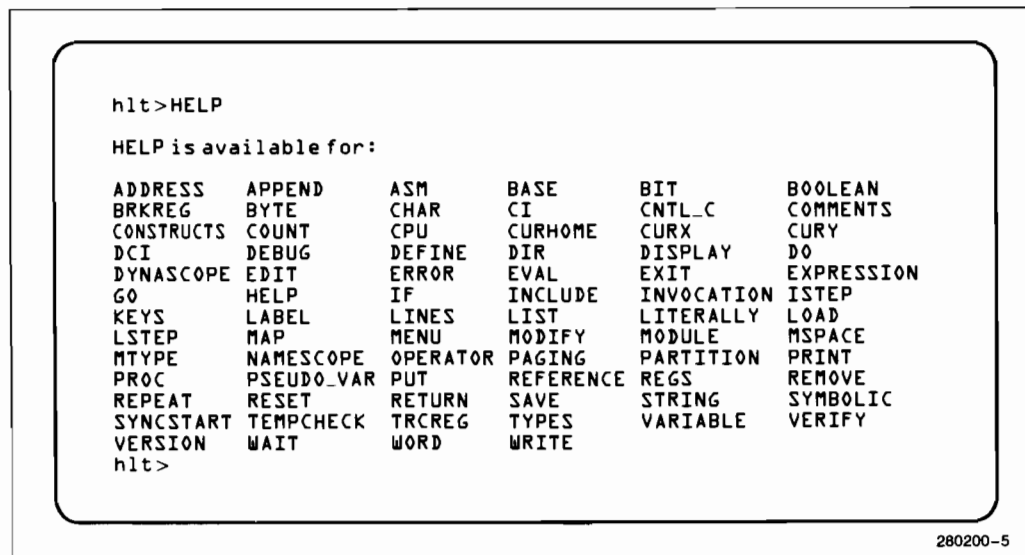
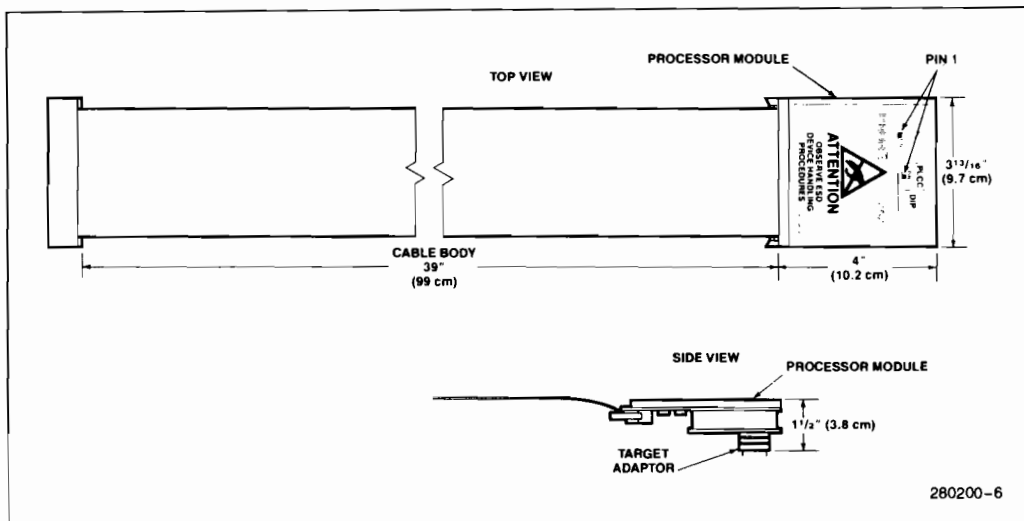


Figure 4. HELP Menu


Figure 5. Processor Module Dimensions

ELECTRICAL CONSIDERATIONS

The emulation processor's user-pin timings and loadings are identical to the 80C252 component except as follows.

Maximum Operating ICC and Idle ICC (ma)*

V _{CC}	Maximum Operating ICC (ma)*			Maximum Idle ICC (ma)*		
	4V	5V	6V	4V	5V	6V
Frequency						
0.5 MHz	0.87	1.62	3.0	0.58	1.21	2.5
3.5 MHz	4.8	6.82	9.76	2.2	4.97	6.33
8.0 MHz	10.5	15.0	20.5	6.0	8.98	11.76
12.0 MHz	15.2	22.2	30.2	9.2	13.34	17.46
16.0 MHz	19.4	28.6	38.7	11.8	17.4	23.4

* ICC is measured with all output pins disconnected.

XTAL1 driven with TCLCH, TCHCL = 10ns, V_{IL} = V_{SS} + .5V, V_{IH} = V_{CC} - .5V. XTAL2 not connected.

For maximum operating ICC

E_A = RST = Port0 = V_{CC}.

For maximum idle ICC

E_A = Port0 = V_{CC}, RST = V_{CC}, internal clock to PCA gated off.

- Up to 25 pf of additional pin capacitance is contributed by the processor module and target adaptor assemblies.
- Pin 31, E_A, has approximately 32 pf of additional capacitance loading due to sensing circuitry.
- Pins 18 and 19, XTAL1 and XTAL2, respectively, have approximately 15 to 16 pf of additional capacitance when configured for crystal operation.

Table 2. CHMOS and HMOS Design Differences

Chip Function	HMOS Component 8031	CHMOS Component 80C31
RST trigger threshold	2.5V	70% Vcc (3.5V @ Vcc = 5V)
RST input impedance	4K — 10K ohms	50K — 150K ohms
Port I _{ij}	— 800μA	— 50 μA
Clock threshold	2.5V	70% Vcc (3.5V @ Vcc = 5V)

Emulating HMOS Components

The ICE-5100/252 emulator is based on a CHMOS emulation processor. There are minor differences between how the ICE-5100/252 emulator supports CHMOS and HMOS designs as shown in Table 2.

Refer to the *Microcontroller Handbook*, order number 210918, for further information on CHMOS and HMOS design considerations.

HOST REQUIREMENTS

- IBM PC AT or PC XT (or PC-DOS compatible) with 512 KB of RAM and a hard disk running under the DOS 3.0 (or later) operating system.
- Intellec Series III/IV Microcomputer Development System running under the ISIS or iNDX operating system respectively, with at least 512 KB of application memory resident.

Disk drives — Dual floppy or one hard disk and one floppy drive required.

ICETM-5100/252 SYSTEM SOFTWARE PACKAGE

- ICE-5100/252 emulator software
- ICE-5100/252 confidence tests
- ICE-5100/252 tutorial software

EMULATOR PERFORMANCE

Memory

Mappable full-speed emulation code memory	64 KB	Mappable to user or ICE-5100/252 emulator memory in 4 KB blocks on 4 KB boundaries.
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Trace Buffer	254- by 24- bit frames
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Virtual Symbol Table

A maximum of 61 KB of host memory space is available for the Virtual Symbol Table (VST). The rest of the VST resides on disk and is paged in and out as needed.

PHYSICAL CHARACTERISTICS

Controller Pod

Width	8¼" (21 cm)
Height	1½" (3.8 cm)
Depth	13½" (34.3 cm)
Weight	4 lbs (1.85 kg)

User Cable

The user cable is 3 feet (approximately 1 m).

Processor Module

(with the target adaptor attached)

Width	3⅜" (9.7 cm)
Length	1½" (3.8 cm)
Height	1½" (3.8 cm)

Power Supply

Width	7 ⁵ / ₈ " (18.1 cm)
Height	4" (10.06 cm)
Depth	11" (27.97 cm)
Weight	15 lbs (6.1 kg)

Serial Cable

The serial cable is 12 feet (3.6 m).

ELECTRICAL CHARACTERISTICS

Power Supply

100 - 120V or 200 - 240V (selectable)
50 - 60 Hz
2 amps (AC max) @ 120V
1 amp (AC max) @ 240V

ENVIRONMENTAL CHARACTERISTICS

Operating temperature	+10° C to +40°C (50°F to 104°F)
Operating humidity	Maximum of 85% relative humidity, non-condensing

ORDERING INFORMATION

Emulator Hardware and Software

Order Code	Description
pl252KITAD	This kit contains: ICE-5100/252 user probe assembly, power supply and cables, serial cables, target adaptor, CPA, ICE-5100 controller pod, software, and documentation for use with an IBM PC AT or PC XT. The kit also includes the 8051 Software Development Package and the AEDIT text editor for use on DOS systems. [Requires software license.]
pl252KITD	This kit is the same as the pl252KITAD kit excluding the 8051 Software Development Package and the AEDIT text editor. [Requires software license.]

pl252KITAS	This kit contains the ICE-5100/252 user probe assembly, power supply and cables, serial cables, target adaptor, CPA, ICE-5100 controller pod, software, and documentation for use with Intel hosts (Series III, IV). The kit also includes the 8051 Software Development Package and the AEDIT text editor for use on Series III/IV. [Requires software license.]
pl252KITS	This kit is the same as the pl252KITAS kit excluding the 8051 Software Development Package and the AEDIT text editor. [Requires software license.]

Software Only

Order Code	Description
pSA252D	This kit contains the host, probe, diagnostic and tutorial software on 5 ¹ / ₄ " disks for use on an IBM PC AT or PC XT (requires DOS 3.0 or later). [Requires software license.]
pSA252S	This kit contains the host, probe, diagnostic and tutorial software on 8" disks (both single-density and double-density) for use on a Series III, and on 5 ¹ / ₄ " disks for use on a Series IV. [Requires software license.]

Other Useful Intel Debug and Development Support Products

Order Code	Description
pD86ASM51	8051 Software Development Package (DOS version) — Consists of the ASM-51 macro assembler which gives symbolic access to 8051 hardware features; the RL51 linker and relocator program that links modules generated by ASM-51; CONV51 which enables software written for the MCS-48 family to be up-graded to run on the 8051, and the LIB51 Librarian which programmers can use to create and maintain libraries of software object modules. Use with the DOS operating system (version 3.0 or later).

pD86PLM51	PL/M-51 Software Package (DOS version) — Consists of the PL/M-51 compiler which provides high-level	pI86ASM51	8051 Software Development Package (ISIS version) — Same as the pD86ASM51 package except this one
	programming language support; the LIB51 utility that creates and maintains libraries of software object modules, and the RL51 linker and relocater program that links modules generated by ASM-51 and PL/M-51 and locates the linked object modules to absolute memory locations. Use the DOS operating system (version 3.0 or later).	pI86PLM51	is for use with the Series III. PL/M-51 Software Package — Same as the pD86PLM51 package except this one is for use with the Series III and Series IV.
		pD86EDIEU	AEDIT text editor for use with the DOS operating system.



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*Field Application Location



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